April 21, 1998

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To: Regional Water Management Division Directors

Subject: Permitting Guidance for Semiconductor Manufacturing Facilities

Introduction

Clarification has been requested by semiconductor manufacturing facilities regarding the scope of 40 C.F.R. Part 469, Electrical and Electronic Components Point Source Category, and 40 C.F.R. Part 433, Metal Finishing Point Source Category. Currently, semiconductor manufacturing facilities are regulated by Subpart A of Part 469, and may also have certain unit operations regulated by Part 433. Apparently there have been inconsistent approaches used by permitting authorities with regard to when to apply 469 and 433 requirements to the semiconductor manufacturing process. There have also been concerns raised about the applicability of the guidelines considering the pace of advancements and the introduction of new technologies in the semiconductor industry. This guidance is intended to provide an overview of the semiconductor manufacturing process, discuss the overlap between Parts 469 and 433, and examine new and emerging manufacturing technologies and how these processes fit into the regulatory framework of Parts 469 and 433. A more complete discussion of these issues can be found in Attachment 1.

Semiconductor Manufacturing Processes

Semiconductor manufacturing, for the purposes of this guidance, can be grouped into three categories: (1) crystal wafer growth and preparation; (2) semiconductor fabrication (also referred to as wafer fabrication); and (3) final assembly. The semiconductor fabrication processes are typically performed in a clean room and include the following steps: oxidation, lithography, etching, doping (through processes such as vapor phase deposition and ion implantation), and layering (through processes such as metallization). During the fabrication process, wafers may be cycled through several of these steps and some of the steps may be repeated for various purposes at different points in the process.

The final step in the manufacture of semiconductors consists of assembly and packaging of the semiconductor for final product. In assembly and packaging, the chips proceed from one operation to the next, undergoing each operation only once, though the order of processes depends on the package type and other factors. Semiconductor assembly and packaging processes include wafer separation and sorting, mounting and bonding of the semiconductor to the appropriate mount media, electrically interconnecting the semiconductor to the package, and final package preparation.

Emerging Technologies

Certain semiconductor manufacturers have recently begun performing a Controlled Collapse Chip Connection (C4) electroplating process to add selective thin metal deposits to the surface of the wafer to act as connection points during wafer fabrication. According to industry personnel, this process is required to allow for increased connection points caused by decreased circuit size (hence an increase in the number of devices per semiconductor).

Several semiconductor manufacturers recently began performing a new process for using copper to replace aluminum in microprocessors during wafer fabrication, enhancing electron migration and reducing the width of the circuitry. These sites use a copper metallization process, in which copper is applied with an electroplating operation followed by a rinse. The process deposits a microscopic layer of copper on selected (i.e., circuitry) portions of the wafer.

Both of these processes are part of a sequence of photolithography, etching, and copper deposition processes performed in a clean room environment.

Conclusion

There are new, emerging technologies involved in semiconductor wafer fabrication which involve electroplating type operations. In these operations, metal is applied with an electroplating operation followed by a rinse which may lead permitting authorities to believe the 40 CFR Part 433 regulations should apply. However, as described above, due to emerging wafer fabrication technologies the electroplating operations in wafer fabrication and electroplating operations regulated by 40 CFR Part 433 can be distinguished:

- In the wafer fabrication process, electroplating type operations add microscopic amounts of metal to selective portions of the wafer to enhance the circuitry and decrease wafer size.
- In the final assembly and packaging process, metal layers are applied electrolytically through an electroplating process in which the packages are mounted on racks. Each lead connects to an electric potential to provide contact points for final assembly. The racks are placed in the electroplating solution, where the metal is applied. This process is followed by a rinse. This is typical of the electroplating processes considered in the development of the Part 433 regulation.

After carefully reviewing both the Part 469 and 433 regulations and their associated background documents; examining past regulatory interpretations; visiting semiconductor manufacturing facilities; speaking with the industry; and reviewing current articles and books on the processes, the Agency believes that semiconductor manufacturing can be broken into two sections for the purposes of applying the requirements of 40 CFR Parts 469 and 433. The first section is the wafer fabrication process and the second section is the final assembly and packaging process. The Agency believes that the metal finishing requirements contained in part 433 only cover the process after wafer fabrication which is used to deposit a layer of metal onto the surface of the wafer to provide contact points for final assembly.

April 21, 1998

ATTACHMENT 1

1.0 INTRODUCTION

This report presents an overview of semiconductor manufacturing processes and a discussion of the overlap between the effluent limitations guidelines and standards covering semiconductor manufacturing (Subpart A of the Electrical and Electronic Component Point Source Category at 40 CFR 469.10) and those covering metal finishing operations (the Metal Finishing Point Source Category at 40 CFR 433). This report focuses on new and emerging manufacturing processes used by semiconductor manufacturing facilities and how these processes fit into the regulatory framework established by EPA under 40 CFR 469 and 40 CFR 433.

Section 2.0 of this report presents a summary of semiconductor manufacturing processes, including the new and emerging processes. Section 3.0 presents a summary of three site visits conducted by EPA at semiconductor fabrication facilities. Section 4.0 presents a discussion of the applicability of 40 CFR 469 and 40 CFR 433 and the overlaps between these two effluent guidelines. Section 5 presents a list of references used in preparing this report.

2.0 SEMICONDUCTOR MANUFACTURING PROCESSES

Semiconductor manufacturing processes can be broadly grouped into three main process areas: silicon crystal growth and wafer preparation, semiconductor fabrication, and semiconductor assembly and packaging. The silicon crystal growth and wafer preparation processes consist of growing silicon crystal ingots from which silicon wafers are produced. The ingots are shaped using grinding and cutting tools, and the wafers are sliced from the ingot. Chemical etching and polishing steps are then performed to remove wafer damage and contamination from the grinding and cutting steps, and provide the final smooth surface where device features can be photoengraved. Section 2.1 presents a more detailed description of this process.

Semiconductor fabrication processes are performed to impart various devices into the semiconductor. These processes are typically performed in a clean room environment and include vapor phase metal deposition, lithography, ion implantation, etching, and metalization. Emerging manufacturing processes performed during fabrication include a lead “bump” process to provide more connection points from the semiconductor and a copper metalization process to deposit additional metal layers on the semiconductor. Section 2.2 presents a more detailed description of the semiconductor fabrication processes. Semiconductor assembly and packaging processes include wafer separation and sorting, mounting and bonding of the semiconductor to the appropriate mount media, electrically connecting the semiconductor to the package, and final package preparation. Section 2.3 presents a more detailed description of semiconductor assembly and packaging processes.

2.1 Silicon Crystal Growth And Wafer Preparation

Wafers, which consist of thin sheets of crystalline material, are the starting point for semiconductor production. Wafers may be manufactured at the semiconductor manufacturing facility or purchased separately from a wafer manufacturer.

Silicon, in the form of ingots, is the primary crystalline material used in the production of 99 % of all semiconductors. Several techniques are available to grow silicon crystal ingots from seed crystals. Most semiconductor manufacturers obtain single crystal silicon ingots from other firms (1).

In the first step of wafer preparation, ingots are shaped into wafer form through a series of cutting and grinding steps, usually performed using diamond-tipped tools. The ends of the silicon ingots are removed and individual wafers are cut from the ingot. The wafers may then be polished using an aluminum oxide/glycerine solution to provide uniform flatness in a process called lapping.

This initial shaping of the wafers leaves imperfections in the surface and edge of the wafers that are removed in an etching step. Chemical etching involves the use of hydrofluoric, nitric, or acetic acids as well as alkaline solutions of potassium or sodium hydroxide.

A final polishing step is performed to provide a smooth surface for subsequent processing. In this step, wafers are mounted on a fixture, pressed against a polishing pad under high pressure, and rotated relative to the pad. A polishing slurry, typically containing silicon dioxide particles in sodium hydroxide, is used. This step is both a chemical and mechanical process; the slurry reacts chemically with the wafer surface to form silicon dioxide, and the silica particles in the slurry abrade the oxidized silicon away.

In some cases, silicon wafers are ultrasonically cleaned in potassium chromate or other mild alkaline solutions (1). In the final wafer preparation step, the wafers are usually rinsed in deionized water and dried with compressed air or nitrogen (1).

2.2 Wafer Fabrication

Wafers are usually fabricated in batches of 25 to 40 (1). The wafer fabrication process includes the following steps: oxidation, lithography, etching, doping, and layering. During the fabrication process, wafers may be cycled through several of these steps and some of the steps may be repeated for various purposes at different points in the process. Between any of these steps, contaminants are cleaned off the wafer using either spray or immersion solutions of acids, bases, or organic solvents.

2.2.1 Oxidation

During oxidation, a silicon dioxide layer is grown on the wafer to provide a base for the lithography process. This layer also serves to insulate and protect the wafer during subsequent

processing. Oxidation processes may be dry or wet, and occur in high-temperature furnaces (e.g., >600°C). In the furnace, the silicon wafer surface oxidizes with steam (i.e., wet oxidation) or a gas such as oxygen (i.e, dry oxidation) to form a silicon dioxide layer. In the dry oxidation process, a chlorine source (chlorine gas, anhydrous hydrochloric acid, or trichloroethylene) may be used to alter oxide characteristics.

2.2.2 Lithography

Lithography is the process of imaging a circuit pattern onto a wafer. Lithography requires resolution of less than 1 micrometer. This multistep process is typically accomplished by the use of a photomask with a thin layer of light-sensitive resist material applied to the wafer. The resist is typically spun onto the wafer and baked to remove any solvent remaining in the resist material. The photomask is a glass emulsion plate with a circuit design on top of it made with a hard-surface material (e.g., chromium, chromium oxide, iron oxide). Light is projected through the voids in the photomask that causes the mask pattern to become imaged on the wafer.

One of three types of lithography is typically used: optical, electron beam, or X-ray. Each type has specific advantages and disadvantages depending on the device type and stage of the manufacturing process. The majority of applications are optical systems using ultraviolet (UV) light. The description given below is for a UV system, but other systems use a similar process.

In an optical system, the resist is exposed to UV light through the photomask that contains the circuit pattern. The resist either polymerizes (hardens) when exposed to light (if a negative resist is used) or unpolymerizes (if a positive resist is used). After exposure, the wafer is developed in a solution that dissolves the excess resist and is then rinsed to remove excess developer solution. The majority of development processes use liquid immersion or spray methods, but dry plasma methods are also used. The resulting wafer has a silicon dioxide layer exposed for the circuit pattern, with the rest of the wafer being covered with the remaining resist coating.

Electron-beam systems result in greater resolution than optical systems and can be used to apply a circuit pattern directly on a wafer without resist. Electron-beam systems are typically used to create the photomasks used in optical systems. X-ray systems also result in greater resolution than optical systems, but are not widely used in manufacturing applications (2).

2.2.3 Etching

After the unreacted resist is removed, the wafer is placed in a solution that etches the exposed silicon dioxide layer but does not remove the resist, creating the circuit pattern in the silicon dioxide layer. This pattern forms areas in which dopants will be applied to provide the required electrical properties. Several etching processes are available.

Wet chemical etching uses acid solutions to etch the exposed layer of silicon dioxide at ambient or elevated temperatures. However, wet etching is ineffective for etching multiple plasma-deposited layers and dry etching techniques have been developed that are effective.

In the most commonly used dry etching technique, plasma etching, dry plasma etches are formed above the target layer by ionizing process gases under a vacuum. Although dry etching usually involves reactive halogenated gases, nonhalogenated gases may also be used. Chemicals used during the dry etching process include chlorine, hydrogen bromide, carbon tetrafluoride, sulfur hexafluoride, trifluoromethane, fluorine, fluorocarbons, carbon tetrachloride, boron trichloride, hydrogen, oxygen, helium, and argon (1). Other dry etching techniques include sputter etching, ion milling, reactive etching, and reactive ion beam etching.

After etching, the remaining photoresist is removed using dry or liquid stripping compounds. The wafers are then cleaned prior to doping.

2.2.4 Doping

To create the desired electronic components (transistors, resistors, etc.), impurities (called dopants) are introduced into the wafer to change the conductivity of the silicon. Dopants are introduced according to the silicon dioxide pattern on the wafer either by diffusion or by ion implantation processes.

In the diffusion process, vaporized metals (i.e., dopants) diffuse into exposed regions of the wafer. Dopant atoms are introduced using either a dopant-containing vapor in high-temperature furnaces (400-1000°C) or a dopant-oxide layer coated on the wafer. Dopants include elements such as arsenic, boron, and phosphorus. Other dopants include aluminum, antimony, beryllium, gallium, germanium, gold, magnesium, silicon, tellurium, and tin (1).

The ion implantation process is a physical deposition process that provides greater control of the number and depth of dopant atoms than does the diffusion process. In the ion implantation process, dopant sources (e.g., metals) are ionized in a vacuum chamber at ambient temperature. The ionized particles are then accelerated to high velocities and imbedded into the wafer by an ion implanter. The strength of the ion implanter determines the process gas usage, which commonly includes arsine, phosphine, and boron trifluoride.

2.2.5 Layering

After the doping process, the wafer may be covered with a layer of material that acts as a conductor (e.g., aluminum), a semiconductor (e.g., silicon), or an insulator (e.g., silicon dioxide), depending upon the chip design. Prior to the layering step, the wafer is cleaned. After a layer is applied, the wafer may undergo the steps previously described to impart additional electrical properties and circuits to the wafer. The primary layering methods available include deposition, metalization, and dielectric and polysilicon film deposition.

Deposition processes are used to apply additional layers of silicon, silicon dioxide, or other materials to the wafer. Deposition processes typically employ epitaxial growth, in which the substrate wafer acts as a seed crystal for the new layer. Dopants may be added to provide electrical properties. Two techniques used for epitaxial growth are chemical vapor deposition (CVD) and molecular beam epitaxy (MBE), with CVD being more common.

During CVD, materials are vaporized in a high-temperature reactant chamber furnace to produce a thin layer on the wafer. Materials that may be used during CVD include silane, silicon tetrachloride, ammonia, nitrous oxide, tungsten hexafluoride, arsine, phosphine, and diborane (1). Another gaseous deposition technique is low-pressure CVD, which uses elevated-temperature vacuum chambers that may use nitrogen, silane, arsine, tetraethylorthosilicate (TEOS), dichlorosilane, ammonia, hydrogen fluoride, and nitrous oxide.

In MBE, silicon and one or more dopants are evaporated and transported to the substrate at high velocity in a vacuum. This process is typically performed at lower temperatures than CVD.

Metalization is a process by which the wafer is coated with thin layers of metal to make circuits. Metalization techniques include evaporation and sputtering. The evaporation method uses high temperatures to vaporize a metal that condenses on the wafer surface. Metals used in metalization include aluminum, platinum, titanium, nickel, chromium, silver, copper, tungsten, gold, and germanium. Evaporation methods include electron-beam evaporation, resistance heating evaporation, and inductive heating evaporation. Argon gas is also used in some operations (1).

In the sputtering process, ionized gas atoms (e.g., argon) chip pieces off a target metal that deposit on the wafer to form a layer. Metals used in sputtering include titanium, platinum, gold, molybdenum, tungsten, nickel, and cobalt. Any unnecessary metals from this process may be removed by solvents or acid solutions.

Dielectric and polysilicon films are deposited onto the wafer to provide conducting regions within the device, electrical insulation between metals, and protection from the environment (2). The most widely deposited films are polycrystalline silicon, silicon dioxide, and silicon nitride. Doping elements such as arsenic, phosphorus, or boron also may be added using this process. Oxygen may be added to polysilicon films to act as a semi-insulating material used for passivating the surface.

After the final layering, the wafer is rinsed in water and the wafer back is mechanically ground. A film of gold may then be applied to the wafer back by an evaporation process.

2.2.6 Emerging Technologies in Wafer Fabrication

Semiconductor manufacturing facilities recently began performing a Controlled Collapse Chip Connection (C4), or "lead bump", electroplating process to add lead bumps to the surface of the wafer to act as connection points. According to industry personnel, this process is required to allow for increased connection points caused by decreased circuit size (hence an increase in the number of devices per semiconductor). This process is followed by a rinse that is shared with other semiconductor fabrication processes in a clean room environment. This process also shares a wet air pollution control device with other semiconductor fabrication processes.

Several semiconductor manufacturers recently began performing a new process for using copper to replace aluminum in microprocessors, enhancing electron migration and reducing the width of the circuitry. These sites use a copper metalization process in which copper is applied with an electroplating operation followed by a rinse. This process is part of a sequence of photolithography, etching, and copper deposition processes performed in a clean room environment. The process deposits a microscopic layer of copper on selected (i.e., circuitry) portions of the wafer.

2.3 Semiconductor Assembly and Packaging

The final step in manufacturing semiconductors consists of assembly and packaging of the semiconductor into the final product. The semiconductors, at this stage called chips or dies, can be mounted onto the surface of a ceramic substrate as part of a circuit, connected directly onto a printed wiring board, or incorporated into a protective package (4). Assembly and packaging consists of backside preparation, die separation and sorting, die attach, wire bonding, inspection, plating, trimming, marking, and final testing (4). In assembly and packaging, the chips proceed from one operation to the next, undergoing each operation only once, though the order of processes depends on the package type and other factors.

Backside preparation consists of wafer thinning and gold deposition. Chips may be thinned through either a physical (i.e., grinding or polishing) or chemical (i.e., etching) removal process. Some chips require the application of a gold layer for subsequent attachment to the package via eutectic techniques. In this case, the gold is usually applied in the fabrication area by evaporation or sputtering (4). After backside preparation, the wafer is separated into individual chips by sawing or scribe-and-break techniques.

After separation, the functioning die are identified, sorted, and placed in carriers for subsequent processing. The die are attached to the package using either a gold-silicon eutectic layer or an epoxy adhesive material. Thin wires are then bonded between the chip bonding pads and the inner leads of the package. The bonded die is inspected for alignment, bond placement, contamination, die-attach quality, and bonding quality (4).

The outer package leads are coated with a conductive layer to improve the solderability into a printed wiring board and to provide a protective coating against oxidation or corrosion. The leads are

coated with either lead-tin solder, tin plate, or gold plate. The lead-tin solder is applied either by dipping the packages into a pot of molten solder or by wave soldering. The tin and gold layers are applied electrolytically through an electroplating process in which the packages are mounted on racks with each lead connected to an electric potential. The racks are placed in the electroplating solution, where the metal is applied. This process is followed by a rinse. The electroplating process (including the rinse) is typically the primary source of process wastewater in the semiconductor assembly and packaging process.

After the conductive layer is applied, the packages go through a trimming operation to separate the leads from supports. The packages are then marked to code information on the outside of the package enclosure, after which they undergo a series of tests, including electrical and environmental.

3.0 SUMMARY OF SITE VISITS

At the request of members of the semiconductor manufacturing industry, EPA and its technical contractor, Eastern Research Group, Inc. (ERG), conducted site visits at three semiconductor manufacturing facilities. The purpose of these visits was to observe operations performed at semiconductor fabrication facilities and to review issues relating to the implementation of 40 CFR 469 and 40 CFR 433 at fabrication facilities that perform electroplating operations.

The first facility was producing 0.25-micron microprocessors for personal computers. This facility receives 6-inch or 8-inch diameter silicon wafers, and performs the fabrication processes previously described. The wafers are sent off site for assembly and packaging processes. At the time of the visit, the facility was evaluating implementing the lead bump process. This facility contains a class 1 clean room (less than one particle per cubic meter) with 300,000 square feet of surface area. The clean room was designed such that large portions (up to half) of the clean room may be closed for construction without hampering production. This allows the facility to continuously upgrade their manufacturing capabilities to reflect newer generation technology. Because of this dynamic nature, the basic utilities servicing the clean room (e.g., power, ultrapure water, and waste and wastewater removal) are flexible. Feed lines and waste removal lines, as well as air pollution control devices, are typically set up to service specific process lines within the clean room. The following types of waste streams are generated in the clean room and segregated for subsequent treatment: hydrofluoric acid wastes, solvents, developing solutions, wastewater with high dissolved solids/low fluoride content, and general wastewater streams. The facility has a water purification system consisting of ion exchange and reverse osmosis. Because of the product specifications, the facility requires ultrapure water in all of their processes. The facility uses counter-flow rinses when possible and does not allow much impurity build-up in the water. The facility treats process wastewater in a neutralization system. The facility also has a specific fluoride removal system for hydrofluoric acid wastes, as well as a solvent recovery system. Effluent from the neutralization system is discharged to a reverse osmosis system purchased by the facility and operated by their publicly owned treatment works (POTW).

The second facility manufactures a variety of semiconductors and microprocessors. The facility receives silicon wafers and performs the fabrication operations described above. No assembly and

packaging operations were observed during the site visit; however, these may be performed on site. The site visit focused on fabrication operations performed to manufacture memory chips, which require fewer operations and metal layers than the microprocessors produced at the first facility. The second facility was constructed in 1955, and is one of the oldest semiconductor manufacturing facilities in the world. The facility has been upgraded several times; the operations observed during the site visit have been in place since the early 1980s. The facility operates eight clean rooms, ranging from class 10 to class 1000, with two of these performing electroplating operations in addition to the fabrication operations described in Section 2.0.

The third facility visited was conducting research into the copper metalization process. The site visit focused on this emerging activity and site personnel provided information pertaining to the copper metalization process.

4.0 APPLICABILITY AND OVERLAP OF 40 CFR 469 AND 40 CFR 433

The applicability statement at 40 CFR 469.10 explains the coverage of the semiconductor discharge requirements by stating:

> The provisions of this subpart are applicable to discharges resulting from all process operations associated with the manufacture of semiconductors, *except sputtering, vapor deposition, and electroplating* (emphasis added).

The preamble to the final rule (48 FR 15382) explains that these process operations are subject to the electroplating and metal finishing requirements at Parts 413 and 433 respectively. The technical support document, however, contains a more detailed description of the applicability of these discharge requirements. The following discussion is based on the document titled Development Document for Effluent Limitations Guidelines and Standards for the Electrical and Electronic Components Point Source Category (Phase I) (EPA 440/1-83/075) and on a regulatory interpretation from Mr. L. Keith Silva, Pretreatment Coordinator for USEPA Region 9, to Mr. John E. Watson, Water Quality Supervisor for the city of Phoenix, Arizona (February 23, 1995).

During the manufacture of semiconductors, material is selectively added and etched on a silicon wafer. Page 4-4 of the Development Document explains that:

> The etchant produces depressions, called holes or windows, where the diffusion of dopants later occurs. Dopants are impurities such as boron, phosphorus and other specific metals. These impurities eventually form circuits through which electrical impulses can be transmitted.

As stated by Mr. Silva in his regulatory interpretation of this issue, this discussion indicates that sputtering, vacuum deposition, and electroplating are regulated under 40 CFR Part 469 when those process operations are associated with the photolithographic-etching-diffusion-oxide process sequence in the semiconductor fabrication process. These operations may occur a number of times depending

on the application of the semiconductor.

Page 4-5 of the Development Document explains that the electroplating and metal finishing requirements apply to those process operations associated with wafer assembly:

> After the diffusion processes are completed, a layer of metal is deposited onto the surface of the wafer to provide contact points for final assembly. The metals used for this purpose include aluminum, copper, chromium, gold, nickel, platinum, and silver. The processes associated with the application of the metal layer are covered by the electroplating or metal finishing effluent limitations and standards.

The Development Document for 40 CFR 469 explains that "the electroplating and metal finishing requirements apply to those process operations that prepare the wafer for final assembly." (5) The document specifically discusses electroplating used to deposit a layer of metal on the surface of the wafer to provide contact points for final assembly. This operation has traditionally been performed in the assembly process, as opposed to the fabrication process, of semiconductor manufacturing.

With the recent development of the copper metalization and lead bump processes (described in Section 2.2), electroplating operations more frequently are performed in the fabrication process. The copper metalization and lead bump operations are electroplating, in which a metal is electrochemically deposited on a substrate, and could potentially be regulated under 40 CFR 433. Both operations are performed in clean room environments, using the same tools (i.e., process sinks) as 40 CFR 469 operations. Both operations share ancillary equipment (e.g., air pollution control scrubbers, cleaning equipment) with 40 CFR 469 operations.

The wastewater discharge rates from the copper metalization and lead bump operations are typically less than 1% of the discharge rates from the 40 CFR 469 operations (6). Since this is generally such a small percentage of the total flow, it may be difficult to demonstrate compliance if both 40 CFR 469 and 433 are used to regulate wastestreams in the wafer fabrication area. In such cases the facilities may have to monitor at the source. For a facility such as the first facility, this would require installing dedicated sinks for electroplating, dedicated ancillary equipment, and dedicated piping systems. Given that the manufacturing processes at the first facility are upgraded every one to two years, this may require complex and costly retrofits or may not be technically feasible.

5.0 CONCLUSION

There are new, emerging technologies involved in semiconductor wafer fabrication which involve electroplating type operations. In these operations, metal is applied with an electroplating operation followed by a rinse which may lead permitting authorities to believe the 40 CFR Part 433 regulations should apply. However, as described above, due to emerging wafer fabrication technologies the electroplating operations in wafer fabrication and electroplating operations regulated by 40 CFR Part 433 can be distinguished:

- In the wafer fabrication process, electroplating type operations add microscopic amounts of metal to selective portions of the wafer to enhance the circuitry and decrease wafer size.
- In the final assembly and packaging process, metal layers are applied electrolytically through an electroplating process in which the packages are mounted on racks. Each lead connects to an electric potential to provide contact points for final assembly. The racks are placed in the electroplating solution, where the metal is applied. This process is followed by a rinse. This is typical of the electroplating processes considered in the development of the Part 433 regulation.

After carefully reviewing both the Part 469 and 433 regulations and their associated background documents; examining past regulatory interpretations; visiting semiconductor manufacturing facilities; speaking with the industry; and reviewing current articles and books on the processes, the Agency believes that semiconductor manufacturing can be broken into two sections for the purposes of applying the requirements of 40 CFR Parts 469 and 433. The first section is the wafer fabrication process and the second section is the final assembly and packaging process. The Agency believes that the metal finishing requirements contained in part 433 only cover the process after wafer fabrication which is used to deposit a layer of metal onto the surface of the wafer to provide contact points for final assembly.

6.0 REFERENCES

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(4) Van Zant, P., 1990. *Microchip Fabrication.* McGraw-Hill Publishing Company, New York, New York

(5) Letter from Mr. Keith Silva, EPA Region IX, to Mr. John Watson, City of Phoenix. February 23, 1995.

(6) Information provided to EPA by the Semiconductor Industry Association. December 16, 1997.